REMARKS

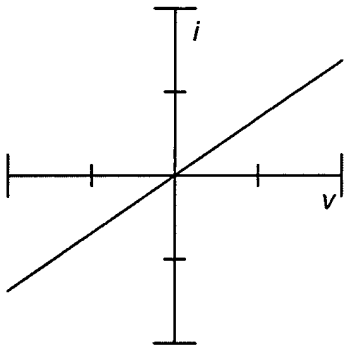
Claims 3, 4, 6, 9, 10, 12, 22 and 23 were examined. All claims were rejected. In response to the above-identified Office Action, Applicants decline to amend any claims, and do not cancel or add any claims. Reconsideration of the rejected claims in light of the following remarks is requested.

I. Claims Rejected Under 35 U.S.C. § 103(a)

The Examiner rejected claims 3, 4, 9, 10, 22 and 23 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,561,383 issued to Rogers ("*Rogers*") in view of U.S. Patent No. 4,258,310 issued to Asakawa *et al.* ("*Asakawa*") and U.S. Patent No. 6,686,300 issued to Mehrotra *et al.* ("*Mehrotra*"). For the reasons discussed below, Applicants believe the references of record fail to support the rejections of these claims.

With respect to claims 3 and 4, the Examiner asserts that the claimed circuit and method are the same as the circuit of *Rogers'* Fig. 1b[1], if only the resistor were replaced with a leaky field effect transistor ("FET") whose gate is tied to a first terminal. While this is true from a topological perspective (*i.e.* the two-terminal resistor could easily be replaced by a three-terminal FET with its gate tied to one of its other terminals), it is not true that the resulting circuit would operate identically, or even in the expected manner.

A resistor has a linear voltage-to-current (v to i) relationship, where the slope of the line depends only on the resistance:



In contrast, a FET connected as claimed will have a non-linear voltage-current relationship, perhaps similar to this:

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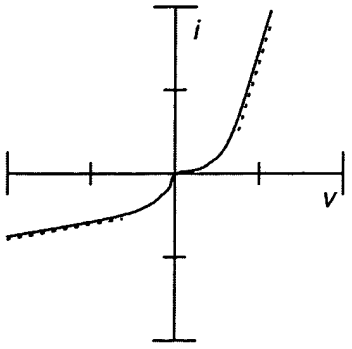
[1] Incidentally, the same circuit is presented as "Prior Art" in Applicants' Fig. 1.



(Note that the exact shape of this curve, and the points at which it crosses the axes, will vary depending on the construction of the device.) The curve in the second graph is fairly linear over certain portions of its range (for example, the portions indicated with dashed lines), while it is decidedly non-linear over other portions. When the FET is operated in a linear portion, it can replace an appropriately-valued resistor. However, if it is operated in another portion of its range, the non-linearity will cause a circuit designed for a resistor to operate differently.

With this background in mind, Applicants turn to the question whether *Rogers'* averaging circuit would operate correctly if a FET was substituted for the resistor. *Rogers* itself offers no assistance and provides no reason why such a change would be made, noting only that the output of the circuit "represents the average of the signal applied to the other end of the resistor." (*See Rogers*, col. 1, lines 34-36.) *Asakawa*, which is relied upon for the teaching that a gate-tied FET can serve as a resistor, also fails to mention the precise conditions under which such a substitution is possible. However, the voltage divider formed by R_1 and R_2 (elements 17 and 18 in *Asakawa*'s Fig. 2) is part of a circuit designed to provide a stable reference voltage (*see* col. 9, lines 42-51), and relies "substantially entirely on the linear relationship between the ratio of the resistances." Thus, even if the "resistors" are not operated in a linear range, their effective resistances must at least have a *ratio* that changes linearly.

In Applicants' circuit, however, only a single gate-tied FET is used, so there is no possibility that nonlinearities in its effective resistance can be ignored as long as a ratio of resistances is constant. Furthermore, Applicants' disclosure explicitly describes the FET operating in both forward-biased and back-biased modes – the range where the *v-i* curve exhibits considerable nonlinearity. Thus, one of ordinary skill would not expect to be able to replace *Rogers'* resistor with a gate-tied FET, and in fact, such a replacement

would produce a circuit whose output voltage is indicative of a local time-average maximum of the input signal voltage, as Applicants claim, and *not* a circuit whose output represents the average of the signal applied to the other end of the "resistor."

The third reference, *Mehrotra*, is relied upon only for a teaching related to the claimed leakage current of the FET, and fails to supply the missing information regarding the operating point of the FET, or to show any flaw in Applicants' analysis of FET-resistor interchangeability.

For at least these reasons, Applicants respectfully submit that *Rogers* and *Asakawa* cannot properly be combined to produce the claimed circuit. The Examiner is requested to withdraw the rejections of claims 3 and 4.

As to claims 9 and 10, those claims recite a circuit and method to produce an output voltage that is a local time-average minimum of an input signal voltage. The claimed circuit is similar to that described by claims 3 and 4 except that the gate of the FET is connected to its *second* terminal, rather than its first. In addition to the arguments presented above in support of claims 3 and 4, which apply with equal force here, Applicants note that yet another reason why *Rogers'* resistor cannot simply be replaced by a gate-tied FET appears. The FET connected as claimed in claims 9 and 10 is essentially the FET of claim 3 with its first and second terminals reversed. However, the circuit of claim 3 produces a *different* output than the circuit of claim 9. A real resistor, in contrast, operates identically regardless of whether it is operated in a "forward" or "reverse" direction. This difference illustrates from another perspective why a resistor cannot be replaced by a gate-tied FET at the unfettered discretion of a designer. For at least these reasons, Applicants respectfully request that the Examiner withdraw the rejections of claims 9 and 10.

As to claims 22 and 23, those claims depend upon claim 3 or claim 9, respectively, and are patentable for at least the reasons discussed above in support of their base claims. Applicants request that the Examiner withdraw these rejections as well.

The Examiner also rejected claims 6 and 12 under 35 U.S.C. § 103(a) as unpatentable over the admitted prior art of Fig. 4 in view of U.S. Patent No. 5,828,603 issued to Pathak ("*Pathak*") and further in view of *Mehrotra* (*supra*).

Claims 6 and 12 recite similar circuits to provide DC offset corrections to an input signal voltage, comprising a number of elements including a FET with a leakage

current in excess of 1μA per micron of device width, wherein the gate is connected to an input port and produces a DC offset correction voltage as a local time-average maximum of the input signal voltage (claim 6); or wherein the gate is connected to an output port and produces a DC offset correction voltage as a local time-average minimum of the input signal voltage (claim 12). The Examiner asserts that *Pathak* shows the equivalence of a FET with its gate connected to a bias voltage and a FET with its gate connected to its source or drain (Fig. 1), but this alleged equivalence is only suggested to be in the context of providing a load ("Z," element 32) as part of the sense circuitry of a non-volatile memory. There is no teaching or suggestion that a leaky FET as claimed, connected as described, would produce either a local time-average maximum or a local time-average minimum of an input signal voltage.

Furthermore, *Mehrota* is relied upon for its alleged teaching of a FET with a leakage current in excess of 1μA per micron of device width. However, that reference does not provide any quantitative values for leakage current per unit of device width, and in fact implies that leakage current is merely an undesirable, albeit unavoidable, consequence of increasing drive current by decreasing gate width (*see* col. 1, lines 48-50). There is no suggestion that increased leakage current, particularly in the specific amount of more than 1μA per micron of device width, would have any useful or beneficial properties.

For at least these reasons, Applicants respectfully submit that claims 6 and 12 are allowable over the references of record, and request that the Examiner withdraw the rejections of these claims.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 3, 4, 6, 9, 10, 12, 22 and 23, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

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Respectfully submitted,
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Lillian Rodriguez — February 15, 2005